



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of: Qiqing C. Ouyang et. al.

02/19/2007

Patent No.: 7,057,216

Serial No.: 10/698,122

Issue date: 06/06/2006

Filed: 10/31/2003

For: **High Mobility Heterojunction Complementary Field Effect Transistors and Methods**
Thereof

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Transmittal for Request of Certificate of Correction

Attached please find form PTO/SB/44 (1 page).

The need for correction is not due to error by the applicant, and would not expect to be charged for Certificate of Correction.

The Commissioner is hereby authorized to charge payment, if needed, of the following fees associated with this communication to Deposit Account No. 50-0510. A duplicate copy of this sheet is enclosed.

Any fees required under 37 CFR 1.20.

Respectfully submitted,

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*Certificate
FEB 27 2007
of Correction*



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CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. : 7,057,216

APPLICATION NO.: 10/698,122

ISSUE DATE : June 06, 2006

INVENTOR(S) : Qiqing Christine Ouyang, Xiangdong Chen

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The text of the ABSTRACT on page 1 is incorrect, and should be replaced in its entirety. Inexplicably, the text of the ABSTRACT is the same as the 2-d paragraph in column 4 of the patent. The text in the submitted application, also as it was published on May 5, 2005 with No.: 20050093021, was correct. The ABSTRACT of the patent should read as follows:

A structure, and method of fabrication, for high performance field effect devices is disclosed. The MOS structures include a crystalline Si body of one conductivity type, a strained SiGe layer epitaxially grown on the Si body serving as a buried channel for holes, a Si layer epitaxially grown on the SiGe layer serving as a surface channel for electrons, and a source and a drain containing an epitaxially deposited, strained SiGe of opposing conductivity type than the Si body. The SiGe source/drain forms a heterojunction and a metallurgical junction with the Si body that coincide with each other with a tolerance of less than about 10nm, and preferably less than about 5nm. The heterostructure source/drain is instrumental in reducing short channel effects. These structures are especially advantageous for PMOS due to increased hole mobility in the compressively strained SiGe channel. Representative embodiments include CMOS structures on bulk and on SOI.

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